

## **REMARKS**

### **Present Status of the Application**

Claims 3, 16 and 17 are objected to because of some informalities.

Claims 1, 2, 4, 5, 6, 12, 13 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Akahori (US 20050012705).

Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US 6,300,928).

Claims 3, 7, 8, 10, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705).

Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705) in view of Kim (US 6,300,928).

Claim 16 is rejected under U.S.C. 103(a) as being unpatentable over Kim (US 6,300,928).

Claims 19-30 are newly added without add new matter to the present application.

### **Discussion of objections to claims**

*Claim 3 recites the limitation "the drives" on line 3 which the examiner suggests be changed to --the drivers--.*

*Claim 16 recites the limitation "the source driver" on line 6 which the examiner suggests be changed to --the gate driver--.*

*Claim 17 recites the limitation "a protocol decoder" which the examiner suggests be changed to --a protocol encoder—because the "decoder" is for encoding as stated*

*later in the claim.*

In response thereto, applicant has changed the limitation “the drives” of claim 3 to “the drivers”, “the source driver” of claim 16 to “the gate driver” and “a protocol decoder” of claim 17 to “a protocol encoder” following the suggestion of the examiner, and reconsideration and withdrawal of the objections are requested.

**Discussion of rejections to claims 1, 2, 4, 5, 6, 12, 13 and 17 under 35 USC 102(e)**

*Claims 1, 2, 4, 5, 6, 12, 13 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Akahori (US 20050012705).*

In response thereto, Applicant has amended claim 1 by incorporation the substance of the subject matter of claim 5 therein, amended claims 2 and 6 to be consisting with the amended claim 1, amended claim 17 to correct some grammatical mistake and make the claim more logical, kept claims 4 and 12 unchanged and canceled claims 5 and 13 without prejudice. Applicant asserts that the pending rejected claims are now patentable, for at least the following reasons:

Independent claim 1, as currently amended, recites in part:

“A serial-protocol panel display system, suitable for use in a panel display apparatus, comprising:

...

**a plurality of gate drivers and source drivers**, used for driving the pixel-array unit to display image; and

a video graphic adapter (VGA) unit, according to a serial protocol, **to export a**

**serial-protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers,**

wherein **the gate and source drivers respectively decode the serial-protocol image display signal**, so as to obtain a plurality of input signals, and to drive pixels of the pixel-array unit” (emphasis added).

Applicant submits that such a serial-protocol panel display system as defined in amended claim 1 is not disclosed, taught or suggested by Akahori, taken alone or in combination with any of the other cited references.

What does Akahori really disclose is that the controller 103 only exports the SDC signals to the source driver 101 (see FIG. 1).

Thus, Akahori fails to disclose a video graphic adapter (VGA) unit of the serial-protocol panel display system **“to export a serial-protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers”** as set forth in amended claim 1.

In addition, due to Akahori only discloses the controller exports the SDC signals to the source driver 101 and supply a scan horizontal sync signal and the like to the gate driver 102. (Paragraph [0029], last four lines). That is, the gate drivers do not receive the serial-protocol image display signal and can not decode the serial-protocol image display signal. Accordingly, Akahori fails to disclose **“the gate and source drivers respectively decode the serial-protocol image display signal”**, as set forth in amended claim 1.

Applicant further submits that the novel physical features of amended claim 1 produce new and unexpected results over Akahori. The video graphic adapter (VGA) unit

of the serial-protocol panel display system of amended claim 1 exports a serial-protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers(see FIG. 4), and the gate and source drivers respectively decode the serial-protocol image display signal. Therefore, the source driver and gate driver can respectively decode out what it needs from the serial-protocol image display signal. In addition, the serial-protocol panel display system of amended claim 1 is relatively simple and is easy to manufacture.

For at least the above reasons, amended claim 1 is submitted to be novel, unobvious, and patentable over Akahori under both 35 U.S.C. 102 and 35 U.S.C. 103. Reconsideration and withdrawal of the rejection of amended claim 1 are requested.

Claims 2, 4, 6 and 12 depend directly from amended claim 1. For the similar reasons as asserted above in relation to amended claim 1, claims 2, 4, 6 and 12 are also novel, unobvious, and patentable over Akahori under both 35 U.S.C. 102 and 35 U.S.C. 103. Reconsideration and withdrawal of the rejections are requested.

Claims 5 and 13 have been canceled without prejudice, therefore the rejections relating thereto are now moot.

Independent claim 17, as currently amended, recites in part:

“A video graphic adapter (VGA), suitable for use in a panel display apparatus to receive image control signals, comprising:

...

**a protocol encoder, coupled with the VGA chip for encoding, and exporting a serial-protocol image display signal and a clock signal”** (emphasis added).

Applicant submits that such a video graphic adapter (VGA) as defined in amended claim 17 is not disclosed, taught or suggested by Akahori, taken alone or in combination with any of the other cited references.

Akahori discloses the controller 103 exports a serial-protocol image display signal and a clock signal(see FIG. 1). However, Akahori does not disclose the controller 103 comprises a protocol encoder and the serial-protocol image display signal and the clock signal are encoded by the controller 103. In other word, the controller 103 of Akahori can directly receive the serial-protocol image display signal and the clock signal from outer circuit. Thus, Akahori fail to disclose the **“VGA comprising a protocol encoder for encoding and exporting a serial-protocol image display signal and a clock signal”** as set forth in amended claim 17.

Applicant further submits that the novel physical features of amended claim 1 produce new and unexpected results over Akahori. The video graphic adapter (VGA) comprising a protocol encoder for encoding and exporting a serial-protocol image display signal and a clock signal. Thus, even signals imports into the VGA is not serial-protocol image display signal, the VGA of the amended claim 17 can transfer the imported signal to serial-protocol image display signal which includes what need to be decoded by the source driver and the gate driver respectively.

For at least the above reasons, amended claim 17 is submitted to be novel, unobvious, and patentable over Akahori under both 35 U.S.C. 102 and 35 U.S.C. 103. Reconsideration and withdrawal of the rejection of amended claim 17 are requested.

**Discussion of rejections to claim 15 under 35 USC 102(b)**

*Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US 6,300,928).*

In response, Applicant respectfully traverse as the following reasons.

Independent claim 15, recites in part:

“A gate driver, suitable for use in a panel display apparatus to drive corresponding pixels, comprising:

...

a gate input interface, **receiving a serial-protocol image display signal and a clock signal**, wherein the serial-protocol image display signal and the clock signal are **continuously transmitted to a next one of the gate driver**, and are used **for decoding out a plurality of gate input signals**”(emphasis added).

Kim discloses the interior configuration of a circuit diagram of a gate driver(see FIG. 4). However, Kim fails to disclose a connecting relationship between two gate drivers. In addition, Kim fails to disclose the gate driver “**receiving a serial-protocol image display signal and a clock signal**, wherein the serial-protocol image display signal and the clock signal are **continuously transmitted to a next one of the gate driver**” as set forth in claim 15.

Furthermore, Kim disclose the gate driver starts to work depending on receiving a STV signal and two clock signals (see FIG. 4) from an outer controller. In contrast, the gate driver of claim 15 can generate the needed STVD and STVU signals by decoding the received serial-protocol image display signal(see FIG. 6). Thus, Kim fails to disclose

such gate driver as set forth in claim 15.

For at least the above reasons, claim 15 is submitted to be novel, unobvious, and patentable over Kim under both 35 U.S.C. 102 and 35 U.S.C. 103. Reconsideration and withdrawal of the rejection of claim 15 are requested.

**Discussion of rejections to claims 3, 7-11, 14, 16 and 18 under 35 USC 103**

*Claims 3, 7, 8, 10, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705).*

Claims 3, 7, 8 and 10 directly or indirectly depend from amended claim 1. Applicant refers to and relies on the above assertions whereby amended claim 1 is unobvious and patentable over Akahori under 35 U.S.C. 103(a). Therefore, claims 3, 7, 8 and 10 are also unobvious and patentable over Akahori under 35 U.S.C. 103(a).

Claim 14 has been canceled without prejudice, therefore the rejections relating thereto is now moot.

Independent claim 18, as currently amended, recites in part:

“A serial-protocol panel display method, comprising:

...

sequentially **transmitting the serial-protocol image display signal and the clock signal to a plurality of source drivers;**

sequentially **transmitting at least a portion of the serial-protocol image display signal and the clock signal to a plurality of gate drivers;**

**decoding the serial-protocol image display signal into a first set of control**

**signals and a color information in each of the source drivers**, used for pixel display;

**decoding the serial-protocol image display signal into a second set of control signals in each of the gate drivers”** (emphasis added).

Applicant submits that amended claim 18 has defined the first and second driver respectively to be the source driver and the gate driver. For reasons similar to those asserted above in relation to amended claim 1, Akahori fails to disclose the method of decoding the serial-protocol image display signal both by the source driver and the gate driver.

Applicant submits that such a serial-protocol panel display method as defined in amended claim 18 is patentable over Akahori under 35 U.S.C. 103(a). Reconsideration and withdrawal of the rejection and allowance of amended claim 18 are requested.

*Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705) in view of Kim (US 6,300,928).*

Claims 9 and 11 directly or indirectly depend from claim 1. Applicant refers to and relies on the above assertions whereby amended claim 1 is unobvious and patentable over Akahori under 35 U.S.C. 103(a). In addition, Kim also fails to disclose the video graphic adapter (VGA) unit of the serial-protocol panel display system **“to export a serial-protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers”** and **“the gate and source drivers respectively decode the serial-protocol image display signal”** as set forth in amended claim 1.

Applicant further submits that the novel physical features of amended claim 1 produce new and unexpected results. The video graphic adapter (VGA) unit of the serial-protocol panel display system of amended claim 1 exports a serial-protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers(see FIG. 4), and the gate and source drivers respectively decode the serial-protocol image display signal. Therefore, the source driver and gate driver can respectively decode out what it needs from the serial-protocol image display signal. In addition, the serial-protocol panel display system of amended claim 1 is relatively simple and is easy to manufacture.

For at least the above reasons, amended claim 1 is submitted to be unobvious and patentable over Akahori in view of Kim under 35 U.S.C. 103(a). Therefore, claims 9 and 11 are also patentable over Akahori in view of Kim under 35 U.S.C. 103(a).

*Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,300,928).*

Claim 16 depend directly from claim 15. Applicant refers to and relies on the above assertions whereby claim 15 is unobvious and patentable over Kim under 35 U.S.C. 103(a). Therefore, claim 16 is also unobvious and patentable over Kim under 35 U.S.C. 103(a).

#### **Discussion of newly added claims 19-30**

The claims 19-30 are newly added according to the description of present

application which shows that “According to a serial protocol, the image control signal is encoded into a serial image display signal. The serial image display signal and the clock signal are sequentially fed into several first drivers. At least a portion of the serial image display signal and the clock signal are sequentially fed to several second drivers.” (Lines 3-8 of paragraph [0015]). Accordingly, the claims 19-30 are newly added without add new matter to present application.

Besides, Akahori fail to disclose “drivers decode the serial-protocol signal, so as to obtain a plurality of **image signals** and **control signals**, and to drive pixels of the pixel-array unit”. The control signals disclosed by Akahori such as the start pulse S and the clock signal C are fed to the drivers in parallel (Fig. 1). That is, Akahori fail to disclose the newly added claim 19 and its dependant claims 20-30. Moreover, Akahori also fail to disclose the newly added claim 19 and its dependant claims 20-30 in view of Kim.

**CONCLUSION**

For at least the foregoing reasons, it is believed that all the pending claims 1-30 of the present application patentably define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date :

June 13, 2008

Respectfully submitted,

Belinda Lee

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office

7<sup>th</sup> Floor-1, No. 100

Roosevelt Road, Section 2

Taipei, 100

Taiwan

Tel: 011-886-2-2369-2800

Fax: 011-886-2-2369-7233

Email: [belinda@jcipgroup.com.tw](mailto:belinda@jcipgroup.com.tw)

[Usa@jcipgroup.com.tw](mailto:Usa@jcipgroup.com.tw)